IN THE CLAIMS

Please amend claims 1-2, 4, 8, 17, 22-27, 35-36, 41, and 46-49 as follows below. Please cancel claims 3, 21, 34, and 45 without prejudice.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

Marked up Claims Listing:

1. (Currently Amended) An apparatus comprising:

a buffer to receive a data stream, wherein data is written to the buffer according to a first clock to store data as two sets on each first clock cycle, each data set storing half of the data written to the buffer per first clock cycle, the buffer configured as a first-in first-out stack;

a character monitor coupled to the buffer to monitor the occurrence of an inter-packet gap in the data stream containing removable filler characters and identify the removable filler characters in the buffer; and

a channel controller configured to read data from the buffer according to a second clock and transmit it over an output channel, the channel controller to skip the transmission of one or more removable filler characters if the first clock is faster than the second clock to match the first and second clock rates.

2. (Currently Amended) The apparatus of claim 1 wherein the buffer stores data in ~~two or~~ more than two sets, each set including one or more characters.

3. (Cancelled)

4. (Currently Amended) The apparatus of claim [[3]] 1 wherein, for each data set in the buffer, the buffer has corresponding flag registers to store information about the data in each set.

5. (Original) The apparatus of claim 4 wherein the data in the flag registers is generated by the character monitor.

6. (Original) The apparatus of claim 4 wherein a flag register to identify whether the data in a set includes one or more removable characters.

7. (Original) The apparatus of claim 1 wherein the channel controller reads data from the buffer in the order in which it was written to the buffer.

8. (Currently Amended) An [[The]] apparatus ~~of claim 1 wherein~~ comprising:

a buffer to receive a data stream, wherein data is written to the buffer according to a first clock, the buffer configured as a first-in first-out stack;

a character monitor coupled to the buffer to monitor the occurrence of an inter-packet gap in the data stream containing removable filler characters and identify the removable filler characters in the buffer; and

a channel controller configured to read data from the buffer according to a second clock and transmit it over an output channel, the channel controller to skip the transmission of one or more removable filler characters if the first clock is faster than the second clock to match the first and second clock rates, the channel controller ~~includes~~ including a read pointer controller, the read pointer controller to access a first, a second, a third, and a fourth data sets stored in the buffer, the first, second, third, and fourth data sets forming contiguous parts of the data stream in

that order with the first data set being first in the data stream and the fourth data set being last in the data stream, wherein in a first mode of operation the channel controller transmits the first and second data sets over the output channel.

9. (Original) The apparatus of claim 8 wherein a buffer overflow condition exists if the first clock writes data to the buffer faster than the second clock reads data from the buffer.

10. (Original) The apparatus of claim 8 wherein if an overflow condition is detected the channel controller seeks a data set marked as removable within an inter-packet gap.

11. (Original) The apparatus of claim 8 wherein if an overflow condition is detected and the first data set is marked as removable, then the channel controller skips transmission of the first data set and transmits the second data set and the third data set in the next second clock cycle.

12. (Original) The apparatus of claim 8 wherein if an overflow condition is detected and the second data set is marked as removable, then the channel controller skips transmission of the second data set and transmits the first data set and the third data set in the next second clock cycle.

13. (Original) The apparatus of claim 8 wherein if an overflow condition is detected and a first data set was previously skipped and the second data set is marked as removable, then on the next clock cycle the channel controller skips transmission of the second data set and transmits the third data set and the fourth data set.

14. (Original) The apparatus of claim 8 wherein if an overflow condition is detected and a first data set was previously skipped and a third data set is marked as removable, then on the next clock cycle the channel controller skips transmission of the third data set and transmits the second data set and the fourth data set.

15. (Original) The apparatus of claim 1 wherein the apparatus is an integrated circuit.

16. (Original) The apparatus of claim 1 wherein the first and second clocks have a maximum rate difference of one cycle per one thousand cycles.

17. (Currently Amended) A method for matching the transmission rates of a first clock to the transmission rates of a second clock comprising:

receiving sets of one or more characters over an input channel synchronized by the first clock;

buffering the sets of characters received;

transmitting the buffered sets of characters over an output channel synchronized by the second clock; [[and]]

skipping transmission of a set of characters marked as removable within an inter-packet gap if an overflow condition is detected;

reading a first, a second, a third, and a fourth data sets, wherein the first, second, third, and fourth data sets are contiguous data segments in that order;

transmitting the first and second data sets on a first cycle of the second clock; and

transmitting the third and fourth data sets on a second cycle of the second clock.

18. (Original) The method of claim 17 wherein the sets of one or more characters are received and buffered per first clock cycle.

19. (Original) The method of claim 17 wherein two sets of one or more characters are transmitted per second clock cycle.

20. (Original) The method of claim 17 wherein a set of one or more characters is marked as removable if it contains one or more filler characters and follows a set of one or more filler characters in the input channel.

21. (Cancelled)

22. (Currently Amended) The method of claim [[21]] 17 wherein an overflow condition is detected if the first clock is faster than the second clock.

23. (Currently Amended) The method of claim [[21]] 17 wherein if an overflow condition is detected and the first data set is marked as removable, then skipping the transmission of the first data set and transmitting the second data set and the third data set in the next second clock cycle.

24. (Currently Amended) The method of claim [[21]] 17 wherein if an overflow condition is detected and the second data set is marked as removable, then skipping the transmission of the second data set, and transmitting the first data set and the third data set in the next second clock cycle.

25. (Currently Amended) The method of claim [[21]] 17 wherein if an overflow condition is detected and a first data set was previously skipped and the second data set is marked as removable, then on the next second clock cycle skipping the transmission of the second data set, and transmitting the third data set and the fourth data set.

26. (Currently Amended) The method of claim [[21]] 17 wherein if an overflow condition is detected and a first data set was previously skipped and the third data set is marked as removable, then on the next second clock cycle skipping the transmission of the third data set, and transmitting the second data set and the fourth data set.

27. (Currently Amended) A rate matching system comprising:

means for receiving an input data stream of one or more character sets over an input channel synchronized by a first clock;

means for buffering the one or more sets of characters;

means for transmitting the buffered data over an output channel as an output data stream synchronized by a second clock; [[and]]

means for removing one or more sets of filler characters from the output data stream if an overflow condition is detected;

means for accessing a first, a second, a third, and a fourth character sets, wherein the first, second, third, and fourth character sets are contiguous data segments of the input data stream in that order; and

means for transmitting the first and second character sets on a first cycle of the second clock.

28. (Original) The rate matching system of claim 27 further comprising:

means for detecting an inter-packet gap within the input data stream.

29. (Original) The rate matching system of claim 27 further comprising:

means for identifying a set of filler characters within an inter-packet gap as deletable characters.

30. (Original) The rate matching system of claim 27 wherein the means for removing one or more sets of filler characters from the output data stream includes means for skipping transmission of a set of characters marked as deletable within an inter-packet gap if the first clock is faster than the second clock.

31. (Original) The rate matching system of claim 30 wherein a set of one or more characters is marked as deletable if it contains one or more filler characters and follows a set of one or more filler characters in the input channel.

32. (Original) The rate matching system of claim 27 wherein two sets of one or more characters are transmitted per second clock cycle.

33. (Original) The rate matching system of claim 27 further comprising:

means for detecting rate differences between the first clock and the second clock.

34. (Cancelled)

35. (Currently Amended) The rate matching system of claim [[34]] 27 further comprising:

means for transmitting the third and fourth character sets on a second cycle of the second clock

36. (Currently Amended) The rate matching system of claim [[34]] 27 wherein an overflow condition occurs when the first clock is faster than the second clock.

37. (Original) The rate matching system of claim 36 further comprising:

means for skipping the transmission of the first character set and transmitting the second character set and the third character set on the first cycle of the second clock if an overflow condition is detected and the first character set is marked as deletable.

38. (Original) The rate matching system of claim 36 further comprising:

means for skipping the transmission of the second character set and transmitting the first character set and the third character set on the first cycle of the second clock if an overflow condition is detected and the second character set is marked as deletable.

39. (Original) The rate matching system of claim 36 further comprising:

means for skipping the transmission of the second character set, and transmitting the third character set and the fourth character set on the first cycle of the second clock if an overflow condition is detected and a previous first data set was skipped and the second data set is marked as deletable.

40. (Original) The rate matching system of claim 36 further comprising:

means for skipping the transmission of the third character set, and transmitting the second character set and the fourth character set on the first cycle of the second clock if an overflow condition is detected and a previous first character set was skipped and the third character set is marked as deletable.

41. (Currently Amended) A machine-readable medium having one or more instructions for matching transmission rates across a single channel which when executed by a processor causes the processor to:

receive data over an input channel synchronized by a first clock;

buffer the data;

transmit the buffered data over an output channel synchronized by a second clock; [[and]]

skip transmission of a data marked as deletable within an inter-packet gap if an overflow condition is detected;

read a first, a second, a third, and a fourth data sets, wherein the first, second, third, and fourth data sets are contiguous data segments in that order; and

transmit the first and second data sets on a first cycle of the second clock.

42. (Original) The machine-readable medium of claim 41 wherein two sets of data of one or more characters are received and buffered per first clock cycle.

43. (Original) The machine-readable medium of claim 41 wherein a data set of one or more characters is marked as deletable if it contains one or more idle characters and follows a data set of one or more idle characters in the input channel.

44. (Original) The machine-readable medium of claim 41 wherein the one or more idle characters are removable characters.

45. (Cancelled)

46. (Currently Amended) The machine-readable medium of claim [[45]] 41 further comprising one or more instructions which when executed by a processor causes the processor to:

skip transmission of the first data set and transmit the second data set and the third data set in the first cycle of the second clock if an overflow condition is detected and the first data set is marked as deletable.

47. (Currently Amended) The machine-readable medium of claim [[45]] 41 further comprising one or more instructions which when executed by a processor causes the processor to:

skip transmission of the second data set and transmit the first data set and the third data set in the first cycle of the second clock if an overflow condition is detected and the second data set is marked as deletable.

48. (Currently Amended) The machine-readable medium of claim [[45]] 41 further comprising one or more instructions which when executed by a processor causes the processor to:

skip transmission of the second data set and transmit the third data set and the fourth data set on the first cycle of second clock if an overflow condition is detected and a previous first data set was skipped and the second data set is marked as deletable.

49. (Currently Amended) The machine-readable medium of claim [[45]] 41 further comprising one or more instructions which when executed by a processor causes the processor to:

skip transmission of the third data set and transmit the second data set and the fourth data set on the first cycle of the second clock cycle if an overflow condition is detected and a previous first data set was skipped and the third data set is marked as deletable.